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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,985	10/29/2001	Stephen John Barlow	491.011US2	1200

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/032,985	BARLOW ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-7,9,13 and 20* is/are rejected.

7)☒ Claim(s) *3,4,8,10-12,14-19 and 21-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/809,498.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/29/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-26 are presented for examination.

2. Claim 25 is objected to because of the following informalities: "said signal". Appropriate correction is required. The "said signal" most likely is directed to the external control line in line 2 of the claim. It is believed to be a minor oversight by applicant. Corrections, such as "a signal on the external control line", "said external control line" , or the like, are suggested to more clearly define the language.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1,2,5-7,9, 13, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over of Chu et al. (4,785,393) in view of Narita et al. (5,293,558)

4. AS to claims 1,5, 7, Chu taught disclosed at least :

a) control means for controlling operations within a processor in accordance with stored program , the program comprising the stored instructions of an instruction set (e.g. see fig.1 [14], see col.7, lines 30-44, see instruction set in col.17, lines 5-25);

b) a plurality of registers for storing calculated values (e.g. see fig.1 [working registers 22] [address register 36]);

c) addressing means [32] operable to perform addressing operation including at least a register [36] for addressing data in a data memory (e.g. see fig.30, col.6, lines 45-52);

d) ALU having input and output of n width (see the 32 bit of ALU in fig.2) being operable to calculate data values in co-operation with the registers;

e) a data register for storing arithmetic result (e.g. see fig.2 [154]);

f) a shifter of interposed between the output of the ALU and the data register [154] with a feedback path to shift the result [32 bit] in response to at least a multiplication, or division (see multiplication and division in col.17, lines 5-25).

5. Chu did not specifically show his data register [154] and the shifter had greater width than the n bits (n=32). However, Narita disclosed a system including a shifter [15] and data register [11] which had width greater than n bit (2n-bit width, see fig.10, col.9, lines 45-65). It would have been obvious to one of ordinary skill in the art to use Narita in Chu for including the shift circuit and data register of greater width as claimed because the use of Narita could provide the processing capability of Chu to adjust to different data format, such as the greater width, thereby increasing the adaptability of the ALU circuit in Chu,, and it could be readily achieved by predefining the greater width of Narita's shifter and data register into the configuration file of Chu, such that the control parameter of the shifter and the register width could be recognized by Chu, and because Chu also disclosed a shifter with a greater width [64 bit] (see fig.2), although not interspersed between he data register and the ALU as claimed, one of ordinary skill in the art should be able to recognize the applicability of the greater width at the output of ALU in order adapt to specific data width requirements in response to different type of arithmetic operations, and for the above reasons , provided a motivation.

6. AS to claim 2, Narita's data reregister also have the pairs of outputs (see fig.10 2n bit width, see also fig.4 14H, 14L for the background teaching).

7. As to claim 6, Chu's address and data were also addressable independently (see the separate address and data buses in fig.1).

8. As to claim 9, Chu was also directed to external control via data storage address space (see address map control in col.7, lines 30-44).

9. As to claim 13, Chu also included interrupt routine (e.g. see col.12, lines 20-31).

10. As to claim 20, Chu was also taught 16 bit length in the background teaching (see col.1, lines 25-36).

11. Claims 3,4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the number of cycles of the arithmetic operations being independent of the values actual multiplied.

12. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the execution of a further instruction until instructions are completely executed.

13. Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the storage of data from the data registers was executed using data path not including the arithmetic unit.

14. Claim 11-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the unidirectional data path between the register outputs and arithmetic input and between the arithmetic output and register input.

15. Claim 14-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the response to the communication request from external circuitry only during predetermined periods during normal controlled operation.

16. Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the instruction decoded differently depending on the signal present on the external control line.

17. Claims 17-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of

the base claim and any intervening claims. None of the prior art of record further teaches the combined features of the sub-divided internal clock states, the plural input lines and functional under control of each stored program, the sampling and latch values for the combinational logic circuit only at the defined state within the instruction cycle.

18. Claim 21-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record teaches the combined features of the prestored linear sequence, the high frequency clock,, the low power consumption to suspend execution, and the ending of the suspension state without execution of instruction stored outside the sequence.

19. Claims 23-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the detailed functional elements and operations of the clock circuit as recited in the claim.

20. Claims 25-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of the external control line, RUN-STEP, and the BRK

instruction which either halt the program or effect no meaningful operation depending on the signal.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Emmons et al. (4,561,066) is cited for the basic teaching of the interpersed shift circuit betweent an arithmetic unit and data register (see fig.4, col.6, lines 26-52).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

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21 Century Strategic Plan

DANIEL H. PAN
PRIMARY EXAMINER
GROUP